


FORM PTO-1390 (REV 10-94)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 10873.589USWO
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (If known, see 37 CFR 1.5) Unknown 09/700940
INTERNATIONAL APPLICATION NO. PCT/JP00/01794	INTERNATIONAL FILING DATE March 23, 2000	PRIORITY DATE CLAIMED March 24, 1999	
TITLE OF INVENTION LSI LAYOUT METHOD			
APPLICANT(S) FOR DO/EO/US SAKIYAMA et al.			
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:			
<p>1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.</p> <p>2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.</p> <p>3. <input checked="" type="checkbox"/> This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).</p> <p>4. <input type="checkbox"/> A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.</p> <p>5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2))</p> <p>a. <input checked="" type="checkbox"/> is transmitted herewith (required only if not transmitted by the International Bureau).</p> <p>b. <input checked="" type="checkbox"/> has been transmitted by the International Bureau.</p> <p>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US)</p> <p>6. <input checked="" type="checkbox"/> A translation of the International Application into English (35 U.S.C. 371(c)(2)).</p> <p>7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))</p> <p>a. <input type="checkbox"/> are transmitted herewith (required only if not transmitted by the International Bureau).</p> <p>b. <input type="checkbox"/> have been transmitted by the International Bureau.</p> <p>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</p> <p>d. <input checked="" type="checkbox"/> have not been made and will not be made.</p> <p>8. <input type="checkbox"/> A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).</p> <p>9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).</p> <p>10. <input type="checkbox"/> A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).</p>			
Items 11. to 16. below concern document(s) or information included:			
11. <input type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.			
12. <input checked="" type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.			
13. <input type="checkbox"/> A FIRST preliminary amendment.			
<input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.			
14. <input type="checkbox"/> A substitute specification.			
15. <input type="checkbox"/> A change of power of attorney and/or address letter.			
16. <input checked="" type="checkbox"/> Other items or information: PCT/IB/304; International Search Report			

U.S. APPLICATION NO (If known, see 37 CFR 1.5) Unknown		INTERNATIONAL APPLICATION NO PCT/JP00/01794		ATTORNEY'S DOCKET NUMBER 10873.589USWO		
09/700940						
17. [X] The following fees are submitted: BASIC NATIONAL FEE (37 CFR 1.492(a) (1)-(5)): Search Report has been prepared by the EPO or JPO.....\$860.00 International preliminary examination fee paid to U.S. Patent and Trademark Office (37 CFR 1.492(a)(1)).....\$690.00 No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)).....\$710.00 Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(3)) paid to USPTO\$1000.00 International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....\$100.00				CALCULATIONS PTO USE ONLY		
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$860.00		
Surcharge of \$130.00 for furnishing the oath or declaration later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$		
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE			
Total claims	4 -20 = 0		X \$18.00	\$0		
Independent claims	2 -3 = 0		X \$80.00	\$0		
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$270.00	\$0		
TOTAL OF ABOVE CALCULATIONS =				\$860.00		
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).				\$0		
SUBTOTAL =				\$860.00		
Processing fee of \$130.00 for furnishing the English translation later than [] 20 [] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				+ \$0		
TOTAL NATIONAL FEE =				\$860.00		
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property				+ \$40.00		
TOTAL FEES ENCLOSED =				\$900.00		
				Amount to be:		
				refunded	\$0	
				charged	\$0	
a. [X] Check(s) in the amount of <u>\$860.00 and \$40.00</u> to cover the above fees is enclosed. b. [] Please charge my Deposit Account No. _____ in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>13-2725</u> .						
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.						
SEND ALL CORRESPONDENCE TO Douglas P. Mueller MERCHANT & GOULD P.O. Box 2903 Minneapolis, MN 55402-0903						
				SIGNATURE 		
				NAME	<u>Douglas P. Mueller</u>	
				REGISTRATION NUMBER	<u>30,300</u>	

DESCRIPTION

LSI LAYOUT METHOD

5 TECHNICAL FIELD

This invention relates to a method for stabilizing the power supply in the LSI design using automatic arrangement wiring of standard cells.

BACKGROUND ART

10 In the last few years, in accordance with the power increasingly consumed by LSI, LSI tends to generate increased power supply noise. Furthermore, due to the market demand to promote electric power saving, LSI with lower voltage also has been developed. With this development, an operating margin against power supply noise in LSI internal circuits tends to be degraded.

15 There is a fear that such an increase in power supply noise of LSI may have negative effects on LSI internal circuits. Examples of such negative effects are: (1) deterioration of operating speed, (2) malfunction of circuits, and (3) system malfunction caused by EMI (Electro Magnetic Interference) noise.

For suppression of noise generated from LSI, it has been common to use a
20 method of arranging a power supply capacity inside LSI. This is because the insertion of power supply capacity makes it possible to reduce the alternating current impedance of power supply and to suppress high-frequency noise.

Furthermore, JP5-21711A discloses a method for stabilizing a power supply, which is achieved by arranging the power supply capacity into sections
25 where functional circuits of LSI do not exist. In addition, JP5-283615A discloses a method of efficiently adding power supply capacity by using capacitance between a power supply and an aluminum wire in LSI.

Generally, in using CMOS (Complementary Metal-Oxide Semiconductor) integrated circuits, a charge-discharge current is generated toward load capacity
30 when switching takes place. FIG. 9 illustrates a circuit diagram of a general CMOS integrated circuit. FIG. 9 illustrates a PMOS (P-channel MOS) transistor switch 91, a NMOS (N-channel MOS) transistor switch 92, a ground electrode 93, a power supply capacitor 94, a load capacitor 95, a power supply (Vdd) pad 96, a power supply (Vss) pad 97, a charge current 98, and a parasitic inductor 99.

35 With reference to FIG. 9, when the PMOS (P-channel MOS) transistor switch 91 is turned on, the charge current 98 (Ivdd) flows from the power supply to the load capacitor 95. When the NMOS (N-channel MOS) transistor switch 92 is

turned on, a discharge current to the ground electrode 93 is generated.

The power supply capacitor 94 has accumulated charge energy. The arrangement of the power supply capacitor 94 into the CMOS integrated circuit makes it possible to provide an electric current (Ic) also from the power supply capacitor 94 in addition to the electric current (Ivdd) supplied from the power supply pad 96. Therefore, the variation of current supply from the power supply (Vdd) pad 96 can be controlled.

However, with the increased development of miniature semiconductor integrated circuits in the last few years, the use of an inductor element (L) of an aluminum wire inside LSI tends to increase. Moreover, in using a general CMOS circuit, the parasitic inductor 99 is generated, and this causes power supply noise. More specifically, the power supply noise (ΔV) can be expressed as:

$$\Delta V = L \times di / dt \quad (\text{Formula 1})$$

In the formula 1, di / dt represents a variation of electric current. It is clear from Formula 1 that an effective approach for reduction of power supply noise (ΔV) is either to reduce the variation of electric current (di / dt) or to reduce the parasitic inductor element L. In other words, the parasitic inductor element L increases in proportion to the length of the aluminum wire, so that it is effective to shorten the power supply line on which a current change takes place.

However, in the conventional method described above, the aluminum wire extending from the switched CMOS gate circuit to the power supply capacity was relatively long, so that the power supply inductor element from the power supply capacity to the switching circuit was increased largely. Therefore, it was difficult to achieve sufficient effectiveness for reduction of power supply noise.

DISCLOSURE OF THE INVENTION

In order to solve the above mentioned problems, it is an object of the present invention to provide a LSI layout method for the LSI design of standard cell type, by which sufficient noise suppression as well as sufficient stabilization of the power supply can be achieved.

To achieve this purpose, the present invention provides a LSI layout method for the LSI design by automatic arrangement wiring of standard cells, characterized in that power supply capacitor cells are provided as one of the standard cells in addition to logic gate cells provided as one of the standard cells; the capacitance value of the power supply capacitor cells is determined so as to correspond to the drive load capacity value of the logic gate cells to which the power supply capacitor cells are to be arranged; and the power supply capacitor

cells are arranged in the vicinity of the logic gate cells.

According to this configuration, the power supply capacitor cells are arranged in the vicinity of the logic gate cells with optimal capacitance values corresponding to the load capacity of the logic gate cells. Thus, noise caused by parasitic inductors can be prevented from increasing, and the power supply noise element can be reduced.

Additionally, in the LSI layout method of the present invention, the capacitance value of the power supply capacitor cells is preferably determined to be substantially twice as large as the drive load capacity value of the logic gate cells. If the capacitance value is determined to be about twice as large as the total load capacity of the logic gate standard cells, the power supply noise can be suppressed to about 1/10 or less of the power supply voltage.

Moreover, in the LSI layout method of the present invention, the power supply capacitor cells preferably are arranged in the vicinity of the logic gate cells, which change simultaneously with clock synchronization. By arranging the power supply capacitor cells in the vicinity of the clock-synchronous logic gates, an area loss can be minimized and the power supply noise can be suppressed efficiently.

Next, to achieve this purpose, the present invention provides a LSI layout method for the LSI design using automatic arrangement wiring of standard cells, characterized in that power supply capacitor cells are provided as one of the standard cells, and that the power supply capacitor cells are arranged in spaces of each block where standard cells are not arranged by automatic arrangement wiring.

According to this configuration, the power supply capacitor is arranged in spaces of each circuit block where standard cells are not arranged (dead space). Thus, the output impedance of power supply can be reduced without increasing the block area, and the power supply noise can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of LSI;

FIG. 2 is a wiring diagram of a block formed by automatic arrangement wiring;

FIG. 3 is a wiring diagram formed by automatic arrangement wiring, provided with power supply capacitor cells in Embodiment 1 of the LSI layout method of the present invention;

FIG. 4 is a diagram for explanation of deciding the optimal power supply

capacity in Embodiment 1 of the LSI layout method of the present invention;

FIG. 5 is an illustrative view of a power supply capacitor in a CMOS semiconductor integrated circuit.

FIG. 6 is an illustrative view of a CTS designed circuit;

5 FIG. 7 is an illustrative view of a block layout formed by automatic arrangement wiring using conventional standard cells;

FIG. 8 is an illustrative view of a block layout formed by automatic arrangement wiring using standard cells in Embodiment 2 of the LSI layout method of the present invention; and

10 FIG. 9 is a block diagram of a conventional CMOS integrated circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiment 1

Hereinafter, a first embodiment of the LSI layout method of the present invention will be described with reference to the accompanying drawings. FIG. 1 is a general LSI block diagram; FIG. 2 is a wiring diagram of Block A formed by automatic arrangement wiring; and FIG. 3 is a wiring diagram formed by automatic arrangement wiring, provided with power supply capacitor cells according to the first embodiment of the LSI layout method of the present invention.

FIG. 1 illustrates LSI 1 and circuit blocks 11 to 13 in a block layout using standard cells. As illustrated in FIG. 2, each block is composed of standard cells, and each block is arranged in a rectangular form. The present invention is characterized in that standard cells 22 composed of merely power supply capacitors are prepared in advance as standard cells. The power supply capacitor standard cells 22 are arranged in accordance with the load capacity of each logic gate standard cell 21, as illustrated in FIG. 3, in the vicinity of logic gate standard cells 21.

Here, the term "vicinity" indicates that the power supply capacitor standard cells 22 are placed adjacent to the respective logic gate standard cells 21, which are used for driving load, and that they are arranged on the same power supply lines. Therefore, when the power supply capacitor standard cells are arranged on different power supply lines, regardless of the closeness of both cells, it is not regarded as being placed in the "vicinity".

35 Since the power supply capacitor standard cells 22 are arranged in the vicinity of the logic gate standard cells 21, a charge current toward a load capacity generated when each logic gate standard cell is switching can be provided for the

most part from the power supply capacitor placed in the vicinity, so that the power supply noise indicated as the power supply inductor element L in Formula 1 can be reduced.

It is generally known that if power supply noise (ΔV) is determined to be about twice as large as the total load capacity of the logic gate standard cells 21, ΔV can be suppressed to about 1/10 or less of the power supply voltage (Vdd). (P. Larsson, "di/dt Noise in CMOS Integrated Circuits.", Analog Integrated Circuits and Processing, An International Journal Vol. 14, pp.113-129, 1997.)

Furthermore, the fact that the noise is 1/10 or less of the power supply voltage means that, seen from another perspective, the noise corresponds to about 1/2 of the voltage value of a CMOS threshold voltage. Thus, the suppression of the power supply noise to 1/2 of the threshold voltage becomes a particularly significant element for securing reliability in LSI operations.

Specifically, as illustrated in FIG. 4 as a cell composition of standard cell type, at the time when an automatic arrangement is executed, drive load capacity of each logic gate (C1+C2) is estimated, and a power supply capacitor standard cell 21 having power supply capacity Cd of at least twice as much as the drive load capacity of each logic gate is placed in the vicinity of each logic gate. In other words, the power supply capacitor standard cell 21 is placed so as to satisfy $C_d > 2(C1+C2)$. This arrangement assures that the power supply noise (ΔV) can be suppressed to at least 1/10 of the power supply voltage in the respective logic gate circuit. As a result, the peak value of the power supply noise in the LSI as a whole can be certified.

As for the structure of the power supply capacitor, an optimal configuration in a CMOS semiconductor integrated circuit is illustrated in FIG. 5. More specifically, in a p-sub wafer, a n-well is fixed to Vss and a polysilicon gate electrode is fixed to Vdd. The potential of the gate electrode is determined to be forward bias against the n-well, so that depletion layer capacitance is not produced. Therefore, in spite of its small area, a power supply capacitor having a large capacitance value can be realized.

On the other hand, the arrangement of the power supply capacitor standard cells 22 to all the logic gates creates a large area loss. Furthermore, the power supply noise reaches its peak value when a plurality of logic gates switch simultaneously. Generally, in LSI which operates according to a complete clock-synchronous pattern, a large number of logic gates switch when the clock starts. This is because all the DFF (D Flip-Flop) are designed to operate at the start of the clock. Moreover, with the acceleration of LSI in recent years, the reduction of

clock skew is desired.

With the foregoing background in mind, a design technique called CTS (Clock tree Synthesis) is more and more standardized. This method is one of those methods that can adjust timing so that phases of all the DFF operations become the same. This timing adjustment can be executed by inverter delays in view of wiring delays. FIG. 6 illustrates a typical example of a LSI design using the CTS method. In FIG. 6, DFF standard cells 23 and inverter standard cells 24 are illustrated. The clock phases of all the DFF standard cells can be adjusted to become the same by changing the size etc. of the inverter according to the load capacity, or by adjusting the number of stage of the inverter delays and so forth.

As a result of the high precision achieved by the CTS method, all the DFF now execute switching simultaneously. The problem of power supply noise is most crucial in such a case. Therefore, in view of the balance to be attained between the area reduction of LSI as a whole and the noise suppression effects, the most effective way is to use the above CTS method only for synchronous type logic gates (DFF gates or inverter gates used for CTS etc.) in arranging the power supply capacitor standard cells 22.

According to the first embodiment described above, power supply capacitor cells are newly prepared in the conventional LSI layout method using standard cells, and the power supply capacitor cells with an optimal capacitance value corresponding to the load capacity of logic gate cells are arranged in the vicinity of the logic gate cells. As a result, power supply noise caused by parasitic inductors can be prevented from increasing, and the power supply noise element can be reduced. Furthermore, when the above method is applied only to clock-synchronous type logic gates, the area loss can be kept to a minimum, and the power supply noise can be suppressed efficiently.

Embodiment 2

Next, a second embodiment of the LSI layout method of the present invention will be described with reference to the accompanying drawings. FIG. 7 is a block layout formed by automatic arrangement wiring using conventional standard cells. As illustrated in FIG. 7, the conventional configuration allows dead spaces 71 to exist, which are empty spaces in blocks where standard cells are not arranged. This is due to the following reason. Each block is composed of a plurality of power supply lines on which standard cells are arranged. Since each power supply line is provided with a different number of standard cells, the width of the block in each power supply line differs accordingly, producing these dead

spaces. In the second embodiment, as illustrated in FIG. 8, the power supply capacitor standard cells 22 are arranged in these dead spaces 71. Accordingly, the power supply capacitor cells can be arranged efficiently without changing the conventional configuration of the block 11 and the total block area.

5 Generally, as the power supply capacitor becomes larger, the output impedance of the power supply is reduced. Therefore, to suppress power supply noise effectively, it is advantageous to arrange as many power supply capacitor cells as possible. On the other hand, the block area is physically limited. The second embodiment makes it possible to add power supply capacitor cells without
10 enlarging the total block area. This embodiment can be realized easily by preparing the power supply capacitor cells 22 as standard cells, calculating the possible number of the power supply capacitor cells 22 to be arranged based on the width of the dead spaces of the power supply and the width of the power supply capacitor cells 22, and arranging as many power supply capacitor cells 22 as
15 possible.

According to the second embodiment described above, the power supply capacitor cells 22 are newly prepared, and the power supply capacitor cells 22 are arranged as much as possible in the dead spaces 71, which always existed in each circuit block when automatic arrangement wiring was executed by the
20 conventional method. As a result, the output impedance of power supply can be reduced without enlarging the total block area, and the power supply noise can be reduced effectively.

Semiconductor integrated circuits designed with the use of this method have the advantages of generating less power supply noise and preventing
25 malfunction of circuits from occurring and so forth. Therefore, by applying this semiconductor integrated circuit to various systems and devices, systems and devices with improved quality can be provided.

Moreover, the embodiments described above are only examples of the present invention and do not limit the present invention thereto. The subject
30 matter of the present invention is only limited by claims.

INDUSTRIAL APPLICABILITY

According to the LSI layout method of the present invention described above, in the conventional LSI design using standard cells, power supply capacitor
35 cells with an optimal capacitance value corresponding to the load capacity of logic gate cells are arranged in the vicinity of the logic gate cells. Thus, compared with the conventional LSI layout method, the L-Element of wires in the power supply

can be reduced, so that the power supply noise can be suppressed effectively.

Furthermore, the LSI layout method of the present invention is applied only to logic gates of clock-synchronous type, so that the area loss can be kept to a minimum, and the power supply noise can be suppressed efficiently.

5 In addition, according to the LSI layout method of the present invention, power supply capacitor cells are arranged in dead spaces which were already available in each circuit block. This configuration enables the reduction of output impedance of power supply without enlarging the total block area and also the reduction of power supply noise.

10

CLAIMS

1. A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, comprising the operations of:
 - 5 providing power supply capacitor cells as one of the standard cells in addition to logic gate cells provided as standard cells,
determining a capacitance value of the power supply capacitor cells so as to correspond to a drive load capacity value of the logic gate cells to which the power supply capacitor cells are to be arranged, and
 - 10 arranging the power supply capacitor cells in the vicinity of the logic gate cells.
2. The LSI layout method according to claim 1, wherein the capacitance value of the power supply capacitor cells is determined to be substantially twice as
15 large as the drive load capacity value of the logic gate cells.
3. The LSI layout method according to claim 1, wherein the power supply capacitor cells are arranged in the vicinity of the logic gate cells which change simultaneously with clock synchronization.
20
4. A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, comprising the operations of:
 - providing power supply capacitor cells as one of the standard cells, and
 - arranging the power supply capacitor cells in spaces of each block where
25 standard cells are not arranged by the automatic arrangement wiring.

ABSTRACT

A LSI layout method for the LSI design of standard cell type is provided, by which sufficient noise suppression of power supply noise as well as sufficient
5 stabilization of power supply can be realized. Power supply capacitor cells are provided as one of the standard cells in addition to logic gate cells provided as one of the standard cells. Next, the capacitance value of the power supply capacitor cells is determined so as to correspond to the drive load capacity value of the logic gate cells, and the power supply capacitor cells are arranged in the vicinity of the
10 respective logic gate cells.

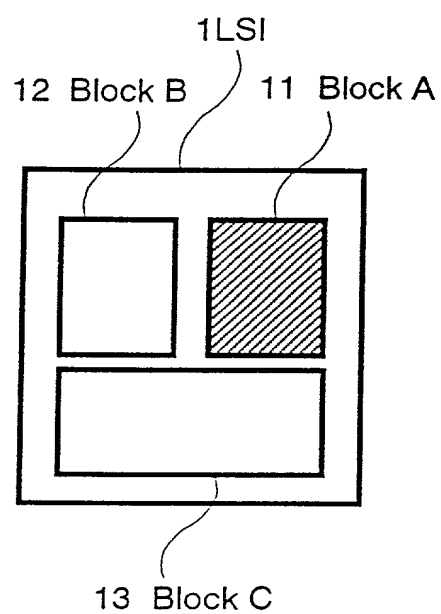


FIG. 1

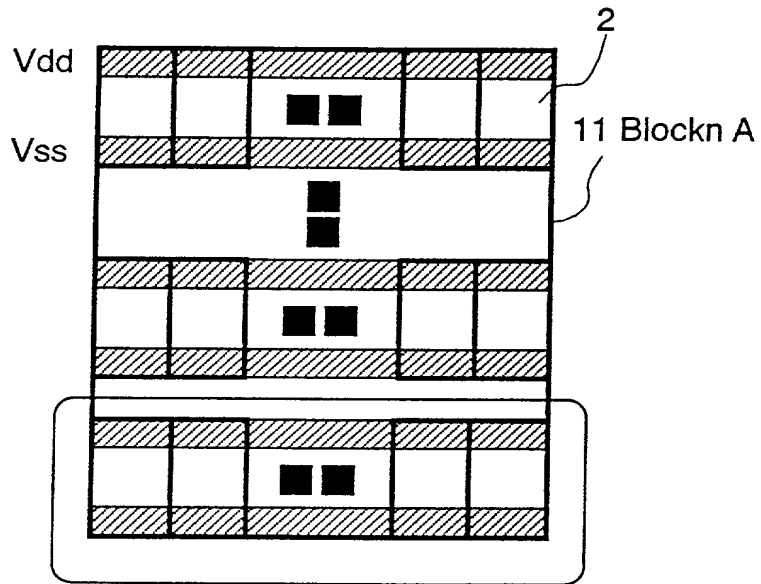
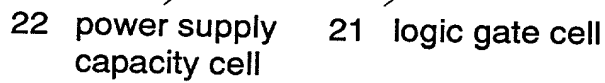


FIG. 2



$\frac{1}{\sqrt{\pi}} \int_{-\infty}^{\infty} f(x) \delta(x-a) dx = f(a)$

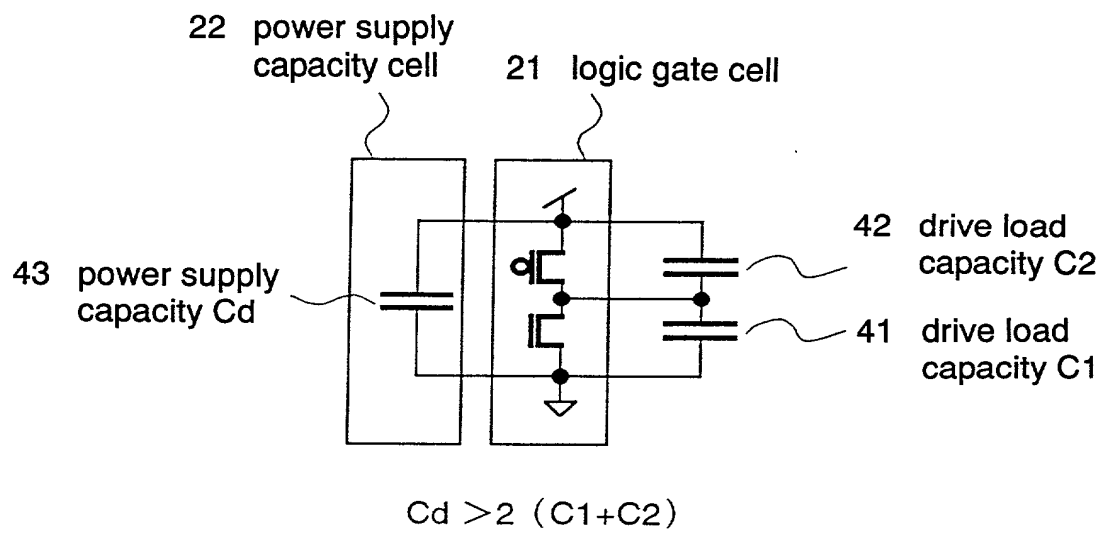


FIG. 4

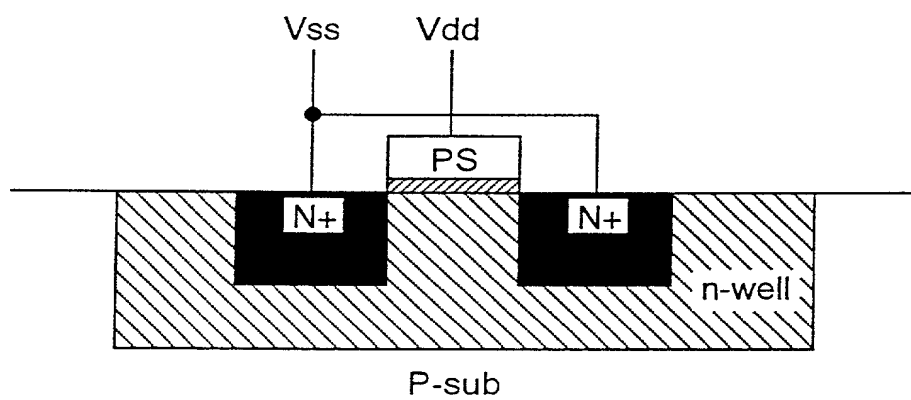


FIG. 5

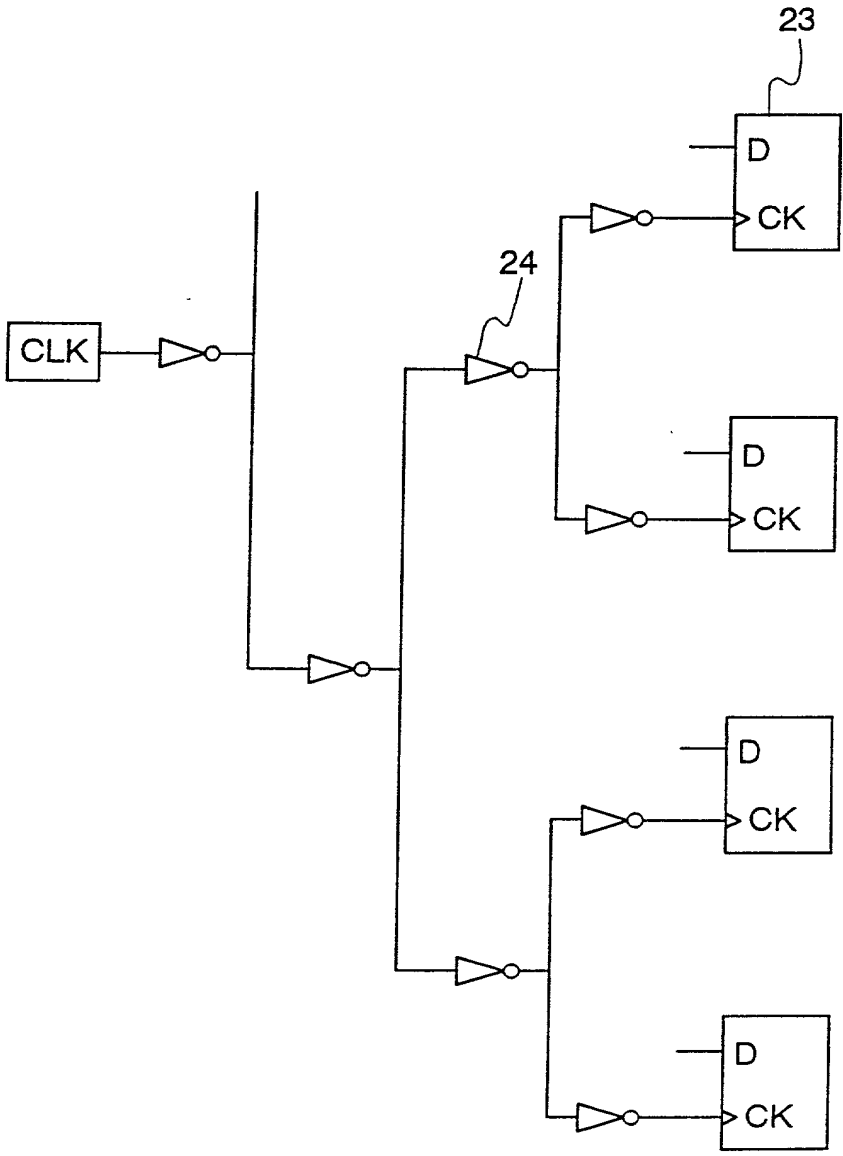


FIG. 6

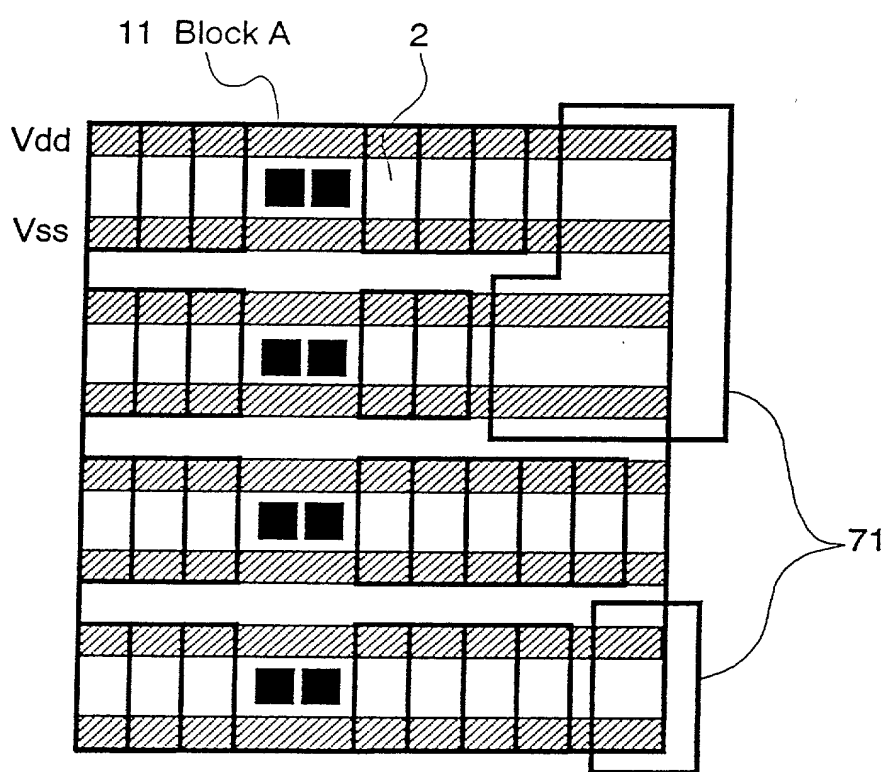


FIG. 7

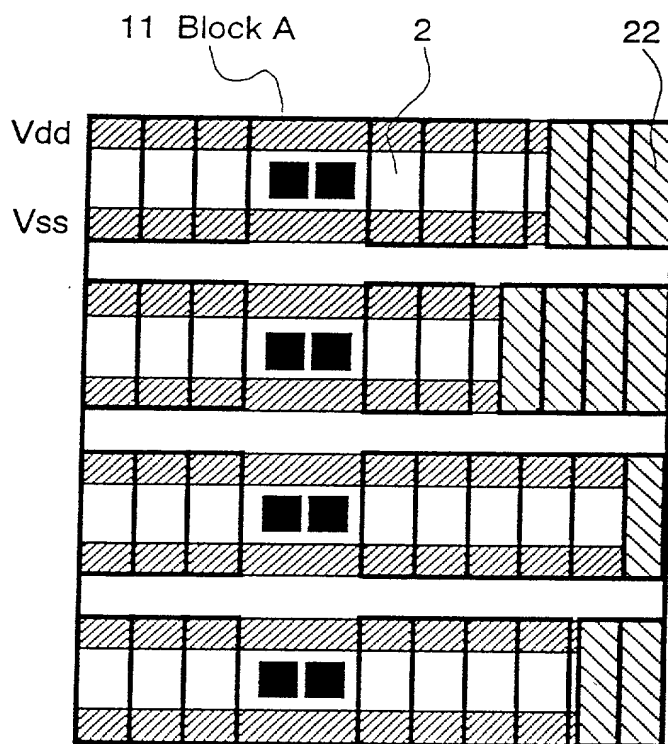


FIG. 8

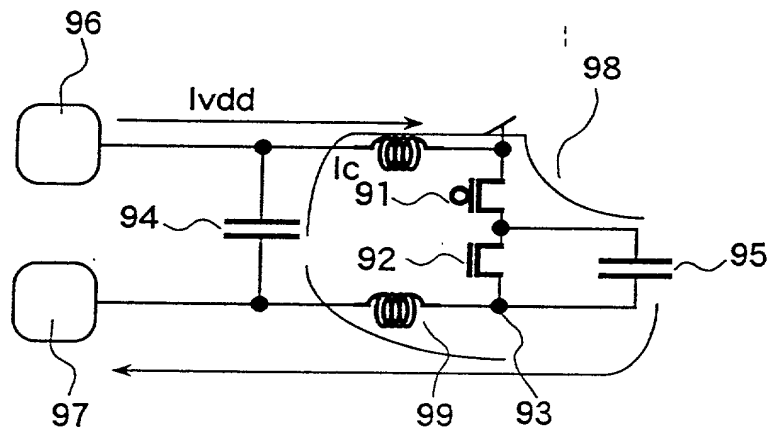


FIG. 9

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:
LSI LAYOUT METHOD

The specification of which

- a. ☐ is attached hereto
b. ☒ was filed on _____ as application serial no. _____ and was amended on _____ (if applicable) (in the case of a PCT-filed application) described and claimed in international no. PCT/JP00/01794 filed on March 23, 2000 and as amended on _____ (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

- a. ☐ no such applications have been filed.
b. ☒ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
Japan	11-079927	24 March 1999	
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Albrecht, John W.	Reg. No. <u>40,481</u>	Kowalchyk, Alan W.	Reg. No. <u>31,535</u>
Ali, M. Jeffer	Reg. No. <u>46,359</u>	Kowalchyk, Katherine M.	Reg. No. <u>36,848</u>
Anderson, Gregg I.	Reg. No. <u>28,828</u>	Lacy, Paul E.	Reg. No. <u>38,946</u>
Batzli, Brian H.	Reg. No. <u>32,960</u>	Larson, James A.	Reg. No. <u>40,443</u>
Beard, John L.	Reg. No. <u>27,612</u>	Liepa, Mara E.	Reg. No. <u>40,066</u>
Berns, John M.	Reg. No. <u>43,496</u>	Lindquist, Timothy A.	Reg. No. <u>40,701</u>
Black, Bruce E.	Reg. No. <u>41,622</u>	Lycke, Lawrence E.	Reg. No. <u>38,540</u>
Branch, John W.	Reg. No. <u>41,633</u>	McAuley, Steven A.	Reg. No. <u>46,084</u>
Bremer, Dennis C.	Reg. No. <u>40,528</u>	McDonald, Daniel W.	Reg. No. <u>32,044</u>
Bruess, Steven C.	Reg. No. <u>34,130</u>	McIntyre, Jr., William F.	Reg. No. <u>44,921</u>
Byrne, Linda M.	Reg. No. <u>32,404</u>	Mueller, Douglas P.	Reg. No. <u>30,300</u>
Campbell, Keith	Reg. No. <u>P-46,597</u>	Pauly, Daniel M.	Reg. No. <u>40,123</u>
Carlson, Alan G.	Reg. No. <u>25,959</u>	Phillips, Bryan K.	Reg. No. <u>P-46,990</u>
Caspers, Philip P.	Reg. No. <u>33,227</u>	Phillips, John B.	Reg. No. <u>37,206</u>
Chiapetta, James R.	Reg. No. <u>39,634</u>	Plunkett, Theodore	Reg. No. <u>37,209</u>
Clifford, John A.	Reg. No. <u>30,247</u>	Prendergast, Paul	Reg. No. <u>46,068</u>
Daignault, Ronald A.	Reg. No. <u>25,968</u>	Pytel, Melissa J.	Reg. No. <u>41,512</u>
Daley, Dennis R.	Reg. No. <u>34,994</u>	Qualey, Terry	Reg. No. <u>25,148</u>
Dalglish, Leslie E.	Reg. No. <u>40,579</u>	Reich, John C.	Reg. No. <u>37,703</u>
Daulton, Julie R.	Reg. No. <u>36,414</u>	Reiland, Earl D.	Reg. No. <u>25,767</u>
DeVries Smith, Katherine M.	Reg. No. <u>42,157</u>	Schmaltz, David G.	Reg. No. <u>39,828</u>
DiPietro, Mark J.	Reg. No. <u>28,707</u>	Schuman, Mark D.	Reg. No. <u>31,197</u>
Edell, Robert T.	Reg. No. <u>20,187</u>	Schumann, Michael D.	Reg. No. <u>30,422</u>
Epp Ryan, Sandra	Reg. No. <u>39,667</u>	Scull, Timothy B.	Reg. No. <u>42,137</u>
Glance, Robert J.	Reg. No. <u>40,620</u>	Sebald, Gregory A.	Reg. No. <u>33,280</u>
Goggin, Matthew J.	Reg. No. <u>44,125</u>	Skoog, Mark T.	Reg. No. <u>40,178</u>
Golla, Charles E.	Reg. No. <u>26,896</u>	Spellman, Steven J.	Reg. No. <u>45,124</u>
Gorman, Alan G.	Reg. No. <u>38,472</u>	Stoll-DeBell, Kirstin L.	Reg. No. <u>43,164</u>
Gould, John D.	Reg. No. <u>18,223</u>	Sumner, John P.	Reg. No. <u>29,114</u>
Gregson, Richard	Reg. No. <u>41,804</u>	Swenson, Erik G.	Reg. No. <u>45,147</u>
Gresens, John J.	Reg. No. <u>33,112</u>	Tellekson, David K.	Reg. No. <u>32,314</u>
Hamer, Samuel A.	Reg. No. <u>P-46,754</u>	Trembath, Jon R.	Reg. No. <u>38,344</u>
Hamre, Curtis B.	Reg. No. <u>29,165</u>	Underhill, Albert L.	Reg. No. <u>27,403</u>
Harrison, Kevin C.	Reg. No. <u>P-46,759</u>	Vandenburgh, J. Derek	Reg. No. <u>32,179</u>
Hertzberg, Brett A.	Reg. No. <u>42,660</u>	Wahl, John R.	Reg. No. <u>33,044</u>
Hillson, Randall A.	Reg. No. <u>31,838</u>	Weaver, Karrie G.	Reg. No. <u>43,245</u>
Holzer, Jr., Richard J.	Reg. No. <u>42,668</u>	Welter, Paul A.	Reg. No. <u>20,890</u>
Johnston, Scott W.	Reg. No. <u>39,721</u>	Whipps, Brian	Reg. No. <u>43,261</u>
Kadievitch, Natalie D.	Reg. No. <u>34,196</u>	Wickhem, J. Scot	Reg. No. <u>41,376</u>
Karjeker, Shaukat	Reg. No. <u>34,049</u>	Williams, Douglas J.	Reg. No. <u>27,054</u>
Kastelic, Joseph M.	Reg. No. <u>37,160</u>	Witt, Jonelle	Reg. No. <u>41,980</u>
Kettelberger, Denise	Reg. No. <u>33,924</u>	Wu, Tong	Reg. No. <u>43,361</u>
Keys, Jeramie J.	Reg. No. <u>42,724</u>	Xu, Min S.	Reg. No. <u>39,536</u>
Knearl, Homer L.	Reg. No. <u>21,197</u>	Zeuli, Anthony R.	Reg. No. <u>45,255</u>

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Merchant & Gould P.C.
P.O. Box 2903
Minneapolis, MN 55402-0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name SAKIYAMA	First Given Name Shiro	Second Given Name
0	Residence & Citizenship	City Osaka	State or Foreign Country Japan	Country of Citizenship Japan
1	Post Office Address	Post Office Address Room 101, Yamaichioowada-Haitsu, 20-20, Kaminoguchi-cho, Kadoma-shi		State & Zip Code/Country Osaka 571-0070/JAPAN
Signature of Inventor 201: Shiro Sakiyama			Date: October 18, 2000	
2	Full Name Of Inventor	Family Name KINOSHITA	First Given Name Masayoshi	Second Given Name
0	Residence & Citizenship	City Osaka	State or Foreign Country Japan	Country of Citizenship Japan
2	Post Office Address	Post Office Address 7-4-2, Kourigaoka, Hirakata-shi		State & Zip Code/Country Osaka 573-0084/JAPAN
Signature of Inventor 202: Masayoshi Kinoshita			Date: October 18, 2000	
2	Full Name Of Inventor	Family Name KAJIWARA	First Given Name Jun	Second Given Name
0	Residence & Citizenship	City Kyoto	State or Foreign Country Japan	Country of Citizenship Japan
3	Post Office Address	Post Office Address 138-8-A-104, Hazukashi-Shimizu-cho, Fushimi-ku, Kyoto-shi		State & Zip Code/Country Kyoto 612-8485/JAPAN
Signature of Inventor 203: Jun Kajiwarara			Date: October 18, 2000	
2	Full Name Of Inventor	Family Name YAMAMOTO	First Given Name Hiroo	Second Given Name
0	Residence & Citizenship	City Osaka	State or Foreign Country Japan	Country of Citizenship Japan
4	Post Office Address	Post Office Address Room 203, Ma-Mezon-YC, 5-21, Tondagaoka-machi, Takatsuki-shi		State & Zip Code/Country Osaka 569-1145/JAPAN
Signature of Inventor 204: Hiroo Yamamoto			Date: October 20, 2000	
2	Full Name Of Inventor	Family Name SATOMI	First Given Name Katsuji	Second Given Name
0	Residence & Citizenship	City Osaka	State or Foreign Country Japan	Country of Citizenship Japan
5	Post Office Address	Post Office Address 4-11-2, Nakamiya, Asahi-ku, Osaka-shi		State & Zip Code/Country Osaka 535-0003/JAPAN
Signature of Inventor 205: Katsuji Satomi			Date: October 18, 2000	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) prior art cited in search reports of a foreign patent office in a counterpart application, and
- (2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim;

or

- (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

- (1) Each inventor named in the application;
- (2) Each attorney or agent who prepares or prosecutes the application; and
- (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.